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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/047,546	01/16/2002	Bjorn Sihlbom	01-521 (4028-01300)	4992

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EXAMINER	
HUYNH, KIM NGOC	

ART UNIT	PAPER NUMBER
2182	

DATE MAILED: 01/19/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/047,546	SIHLBOM ET AL.	
	Examiner	Art Unit	
	Kim Huynh	2182	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-20* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Double Patenting

1. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

2. Claim 1 of U. S. Patent No. 6,667,636 contain(s) every element of claim(s) 1-2 of the instant application and as such anticipate(s) claim(s) 1-2 of the instant application.

"A later patent claim is not patentably distinct from an earlier patent claim if the later claim is obvious over, or **anticipated by**, the earlier claim. In re Longi, 759 F.2d at 896, 225 USPQ at 651 (affirming a holding of obviousness-type double patenting because the claims at issue were obvious over claims in four prior art patents); In re Berg, 140 F.3d at 1437, 46 USPQ2d at 1233 (Fed. Cir. 1998) (affirming a holding of obviousness-type double patenting where a patent application claim to a genus is anticipated by a patent claim to a species within that genus). " ELI LILLY AND COMPANY v BARR LABORATORIES, INC., United States Court of Appeals for the Federal Circuit, ON PETITION FOR REHEARING EN BANC (DECIDED: May 30, 2001).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless -
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

4. Claims 1, 3, 6, 11, 18-20 are rejected under 35 U.S.C. 102(e) as being anticipated by Alasti et al. (US 6,263,390).

Claims 1, Alasti discloses a microprocessor having an internal memory (col 6, ll. 47-50), a DSP 302, a first and second DMA devices coupled to a sharing unit (DMA devices attached to DMA interface 206, see Fig. 2), the sharing unit alternatively coupled the devices to the memory (the I/O gateway 300 and DMA interface 332-334 arbitrate the connection of I/O devices to the bus/memory via DMA interface, see Fig. 2 and the col. 8, ll. 17-22 and col. 9, ll. 12-14) .

Claim 3, Alasti discloses the DSP operates at a first frequency (at 250 Mhz, col. 6, ll. 52-53) and the DMA devices operate at a second frequency slower that the first (memory/bus clock is at 250 Mhz which dictates the maximum clock of the peripheral devices).

Claim 6, Alasti disclose a memory controller (shown in combined with the memory of block 304), in response of the memory transaction request from the devices, provide a control signal indicating the completion of the operation based on the

absent/present of conflict (col. 8, ll. 17-27, DMA interface using tag scheme to indicate pending or completion of the task).

Claim 11, Alasti discloses the claimed invention as discussed in claim 1 and also disclose each of the DMA device operate at different frequency and each will be slower than the DSP and the sharing unit having first and second ports connecting the DMA devices to the memory (channels 510 of Fig. 5) and a third port connecting the DSP to the internal memory (I/O controller coupling to PCI) alternately connecting to the DMA devices in synchronization with the DSP clock frequency (col., 8, ll. 17-24 and 54-60 and col. 9, ll. 12-14, I/O requests are queued in the SRAM 400 but only one is processed at a time based on prioritized arbitration and only one I/O device is connected to the port 502 at a time).

Claim 18 repeats the limitation of claim 6 and is rejected accordingly.

Claims 19-20, the method of claims 19-20 necessitated by the apparatus of claims 1, 3 and 11 above. The multiplexor is the sharing unit described in the apparatus claim and sequentially/alternately couples each of the devices to the memory on a time-multiplexed basis (one I/O device at a time, col. 9, ll. 1-14) on a time multiplexed basis (col. 8, ll. 17-24) in synchronization with a clock timing operation of the DSP.

5. Claims 1-3, 6 and 19-20 are rejected under 35 U.S.C. 102(e) as being anticipated Ozcelik et al. (US 6,041,400).

Ozcelik discloses a microprocessor having a CPU 318 (Fig. 9) plurality of DMA devices (processing core 332, the devices interfacing with the internal memory via

memory controller and DMA, see claim 7) connected to a sharing unit 312 to access internal memory 74, the DMA devices are PLC and coupled to a sharing unit (subswitch 120 alternatively (one at a time, time multiplexed basis) coupled the devices to the memory (see col. 15, claim 12). Please note the system clock dictate all operations of the system and therefore in sync with the system clock.

Ozcelik disclose that the devices being PLC (processing core) and a memory controller 306 for providing a response to indicate the status of the request (Figs. 5-6).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 2 and 13 are rejected under 35 U.S.C 103(a) as obvious over Alasti in view of Ozcelik et al. (US 6,041,400).

Alasti does not disclose the DMA devices being PLC. Ozcelik discloses the use of PLD to implement data processing functions are well known and has becoming the trend in electronic technology in order to improve performance and flexibility of electronic devices (background and col. 1, ll.13-16). It would have been obvious to one having ordinary skill in the art to implement the DMA devices of Alasti using PLC in order to enhance performance and flexibility of his device in line with current trend of technology.

8. Claims 7 and 14 are rejected under 35 U.S.C. 103(a) as obvious over Alasti in view of Amrany et al. (US 6,412,027).

Alasti disclosed the controller having built in arbitration but does not disclose a second sharing unit connected in cascaded configuration with the first. Amrany discloses a cascaded DMA controller configuration to accommodate multiple DMA devices each DMA controller having built in arbitration circuitry to avoid having a separate arbitration circuit (abstract and summary of the invention). It would have been obvious to one having ordinary skill in the art to implement the cascaded DMA controller configuration in order to accommodate for additional DMA devices without requiring a separate arbitration circuit as taught by Amrany.

9. Claims 4-5, 8-10, 12, 15-16 and 18 are rejected under 35 U.S.C. 103(a) as obvious over Alasti or Alasti in view of Armany (with respect to the cascaded DMA configuration).

Alasti does not explicitly teaches the CPU clock to be at 160 Mhz or the DMA devices operate at ¼ of the CPU clock and the sharing unit at ½ of the CPU clock. However, Alasti suggested that the DMA controller can operate at CCLK/N and selected to be multiple of frequencies of the various DMA devices and the DMA devices operates on a divided synchronous clock with respect to the DMA clock (col. 6, ll. 8-35). It would have been obvious to one having ordinary skill in the art at the time the invention was made to vary the value of the CPU frequency and the integer to a desired value as long as it within the capability of the circuit and compatible with the frequencies other devices (bus, memory) in order to simplify the I/O gateway and DMA interface circuit (col. 6, ll.

17-23) . It has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

10. Claim 17 are rejected under 35 U.S.C. 103(a) as obvious over Alasti in view of Amrany and Ozcelik. Claim 17 repeats the limitation the DMA device being PLC of claims 2 and 13 and are therefore rejected accordingly.

11. Claims 3-6, 11-13, 18 are rejected under 35 U.S.C. 103(a) as obvious over Ozcelik in view of Normoyle et al. (US 6,263,390).

Claims 3-5, 11-13, Ozelik does not disclose the CPU clock is higher that the I/O device clock and . However, Normoyle discloses that it is well known that system clock is higher that I/O system clock and each of the device can operate at its own clock different from each other. It would have been obvious to one having ordinary skill in the art to realize that the same principal applies to the multiprocessing IC of Ozcelik in order to be conform with industry standard.

As for the specific value of the CPU of 160 Mhz or the DMA devices operate at ¼ of the CPU clock and the sharing unit at ½ of the CPU clock. Normoyle discloses that the CPU clock is in the range of 132-250 Mhz normally of fixed multiple of the I/O clock which is of 66 or 132 Mhz.

As for the recitation that one device operate at slower frequency that the other, please note it is well know that the speed of various I/O device can be different depending on its application.

As for the device being operate that ¼ of the system clock, the individual devices inherently operates at slower frequency that the interface in order to properly being controlled. It would have been obvious to one having ordinary skill in the art at the time the invention was made to vary multiple integer relative to the frequency of the device and the CPU to a desired value as long as it within the capability of the circuit and compatible with the frequencies other devices (bus, memory) in order to simplify the switching and DMA interface circuit. It has been held that discovering an optimum value of a result effective variable involves only routine skill in the art. *In re Boesch*, 617 F.2d 272, 205 USPQ 215 (CCPA 1980).

12. Claims 7-10 and 14-17 are rejected under 35 U.S.C. 103(a) as obvious over Ozelick in view of Amrany.

Ozelick disclosed the controller having a global switch 304 for handling multiple switches 312-316 each having a plurality of DMA devices but does not disclose a second sharing unit connected in cascaded configuration with the first. Amrany discloses a cascaded DMA controller configuration to accommodate multiple DMA devices each DMA controller having built in arbitration circuitry to avoid having a separate arbitration circuit (abstract and summary of the invention). It would have been obvious to one having ordinary skill in the art to implement the cascaded DMA controller configuration in order to accommodate for additional DMA devices to simplify the arbitration circuit of Ozelick as taught by Amrany.

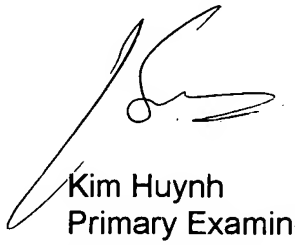
13. Claims 8-10 and 15-17 are rejected under 35 U.S.C. 103(a) as obvious over Ozelick in view of Amrany and further in view of Normoyle . Claims 8-10 and 5-17 repeat the limitation of claims 3-5, 11-13 and therefore is rejected as discussed above.

Conclusion

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kim Huynh whose telephone number is (571) 272-4147.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Kim Huynh
Primary Examiner
Art Unit 2182

KH
1/12/05